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STUDY OF ELECTRONIC TRANSPORT AND BREAKDOWN IN THIN INSULATING FILMS

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Recent progress is reported in an ongoing program of studies of high-field and radiation effects in thin insulating films on semiconducting substrates. The investigations reported here include the generation of interface states in the Si-SiO_2 system by the photoinjection of electrons and by Fowler-Nordheim tunneling of electrons, and a study of radiation-induced interface states. (Keywords!

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1. INTRODUCTION

We report here on recent progress in an ongoing program of research which is directed toward a basic understanding of the electronic properties of thin insulating films and of the interfaces of such films with semiconductors and metals. Of particular interest are the high-field properties of these systems, including charge-carrier injection through the interfaces, electronic transport through the insulators, charge-carrier trapping and recombination at the interfaces and in the insulators, the generation of interface states and of trapping centers, and the mechanisms leading to dielectric breakdown. Phenomena relevant to very large-scale integration are of especial interest. An objective of the program is to provide a rational basis for the choice of materials, processing methods, and treatment of the insulating films in order to obtain the desired performance and reliability. The principal insulating film under study at the present time is silicon dioxide on silicon substrates. We have also studied aluminum oxide, silicon nitride, and high-pressure-grown silicon dioxide. The techniques and apparatus that we have developed under this program are, moreover, immediately applicable to the study of other types of insulator-semiconductor systems.

Chapter 2 of this report is a preprint of a paper by Stella Pang, S.A. Lyon, and Walter C. Johnson entitled "Generation of Interface States in the Si-SiO_2 System by Photoinjection of Electrons." In this paper we describe the results of a study of the interface states that are generated in the Si-SiO_2 system when a photoinjected electron current is passed through the structure, and we give evidence indicating that there are pre-existing centers with a density of about 10^{12} cm^{-2} which are activated by passage (perhaps capture) of electrons. Our data show an interaction cross section of 10^{-18}-10^{-19} cm^2 for the production of an interface state by an electron. In the paper we discuss the experiments and the results, we show that there does not seem to be a strong dependence on either temperature or direction of current, and we give the results of annealing experiments.

Fowler-Nordheim tunneling is being used increasingly as the means of altering the memory state of nonvolatile semiconductor memory cells of the floating-gate type. A progressive change in the write/erase threshold voltage limits the number of write/erase cycles that can be used. Two physical difficulties are observed: electrons are trapped in the insulator, and interface states are generated. While the former has been studied in some detail, comparatively little is known about the latter. In Ch. 3 we give the results of a recent study of interface-state generation associated with Fowler-Nordheim tunneling.

The interface states that develop in the Si-SiO_2 system after holes are trapped at the interface require thermal energy for their generation and do not appear at liquid nitrogen temperature. In contrast with this, the interface states that appear when electrons are passed through the interface are generated even at liquid nitrogen temperature, as is shown by the results presented in Ch. 2 of this report. The relationship, if any, between the two types of interface states is not known. J.K. Wu is conducting a further study of the connection between trapped holes and interface states, and his results up to this time are given in Ch. 4.

The investigations reported here were jointly supervised by Professor Walter C. Johnson and Stephen A. Lyon.

2. GENERATION OF INTERFACE STATES IN THE $Si-SiO_2$ SYSTEM BY PHOTOINJECTION OF ELECTRONS

(Stella Pang, S.A. Lyon, and Walter C. Johnson)

Abstract

The generation of interface states is observed in the $Si-SiO_2$ system when a photoinjected electron current is passed through the MOS structure. The increase in the density of interface states as a function of total charge passed can be fitted by assuming that there are about 10^{12} sites/cm^2 that can interact with the electrons, and that the interaction cross section for production of an interface state by an electron is about 10^{-19}-10^{-18} cm^2. Within sample-to-sample variations, the generation does not appear to be dependent on either the direction of current or the temperature (in the range 97°K-0°C). More than 50% of the generated states are stable for 6 months at room temperature, but they anneal rapidly above 200°C, leaving a residue of electrons trapped near the $Si-SiO_2$ interface.

2.1. Introduction

A number of investigators have measured electron trapping in the oxide layers of Metal-SiO_2-Si structures after large numbers of electrons have been passed through the SiO_2.[1-9] We are reporting the first quantitative study of the interface states generated by electron currents in MOS devices. Using UV light, electrons have been photoinjected from both the Si substrate and the Al field plate to produce an electron current through the oxide at moderate fields. Large numbers of interface states are generated at both 90°K and 0°C. We report here on the observed rate of generation of the states, the effect of bias polarity and temperature during injection, and the annealing properties of the states. Our data indicate that there are preexisting centers with a density of about 10^{12} cm^{-2} which are activated by the passage of electrons. The cross section for this activation process is measured to be 10^{-18}-10^{-19} cm^2. In addition, we note that the interface states produced by electron currents appear to be different from those generated by ionizing radiation. We observe that the former generate immediately at 90°K, while the latter do not appear until the sample is warmed if the irradiation is carried out at liquid-nitrogen temperature.[10-13]

2.2. Sample Preparation and Experimental Techniques

The samples used in our experiments were MOS capacitors with n-type (100) Si substrates of 5-10 ohm-cm resistivity. The oxide films were grown in dry O_2 with 3% HCl at 1000°C for 30 min. Aluminum back contacts were used, and the devices were sintered in H_2 at 450°C for 30 min after Al evaporation. Bias-temperature-stress measurements[14] showed that sodium contamination was negligible.

The interface-state density was measured by a technique proposed by Jenq.[11,15] Two curves are taken at liquid-nitrogen temperature, one with electrons frozen into the interface states and the other with holes frozen into the states. The two C-V curves have parallel portions that differ by a translation along the voltage axis owing to the different amounts of charge at the interface. The method includes all interface states except those so close to a band edge that they can emit their charge carriers during the short time required to record the C-V curve. Measurements requiring a few seconds allow states within 0.2 eV of a band edge to emit their carriers[16] at 90°K; thus, at this temperature, the Jenq technique includes those interface states lying within approximately the central 0.7-eV portion of the silicon bandgap. The number of interface states per unit area is given by $N_{ss} = C_{ox}\Delta V/e$, where C_{ox} is the oxide capacitance per unit area, ΔV is the translation between the two curves, and e is the magnitude of the electronic charge. The application of the method is illustrated by the low-temperature (97°K) C-V curves of Fig. 1. Each curve was taken at a ramp speed of 1.0 V/sec. On the downsweep, electrons are frozen into the interface states in the central region of the Si bandgap. At the leftmost portion of the sweep the sample is illuminated temporarily to supply holes to the interface, after which the upsweep is taken. The horizontal translation between the parallel portions of the curves occurring near $C/C_{ox} = 0.35$ provides the measure of the density of interface states. The shallow ramp of Curve 3 shows a lateral nonuniformity.

Ultraviolet light from a 1 kW xenon arc lamp, together with a field-plate bias providing an average oxide field of 1 MV/cm, produced the electron current in the oxide. A water filter and a Corning 7-54 glass filter were used to cut off the IR and visible light, allowing photons with energies in the range 3.2 - 4.7 eV to pass. The light was focused by an S1-UV quartz lens onto the semitransparent Al electrode. The photoinjection experiments were done at both liquid-nitrogen temperature and at 0°C.

2.3. Generation of Interface States

Figure 2.1 shows typical low-temperature (97°K) C-V curves obtained in the photoinjection experiments. Curve 1 shows the initial condition of a fresh sample. The number of interface states indicated by the Jenq technique is 2×10^{10} cm^{-2}. The sample was then biased, gate positive, to an average field of 1 MV/cm, and was exposed to the UV light while being held at 97°K. The resulting current density was about 1.3 $\mu A/cm^2$. Curve 2 shows the low-temperature C-V curves obtained after photoinjecting 5.4×10^{-2} C/cm^2 through the oxide. The interface density has increased to 2.8×10^{11} cm^{-2}. The photoinjection was continued for a total of 58 hrs, during which time a total charge of 0.24 C/cm^2 passed through the oxide. Curve 3 is the resulting low-temperature characteristic. The interface-state density has increased to 7.9×10^{11} cm^{-2}.

Figure 2.2 is a plot of the number of interface states as a function of charge passed through the SiO_2. The data indicate that initially the number of interface states generated is directly proportional to the total number of electrons passed through the oxide, but that there is a trend toward eventual saturation. The data can be fitted with an equation of the form:

$$N_{ss} = N_{sat}(1 - e^{-\sigma N_{inj}}) \quad , \qquad (2.1)$$

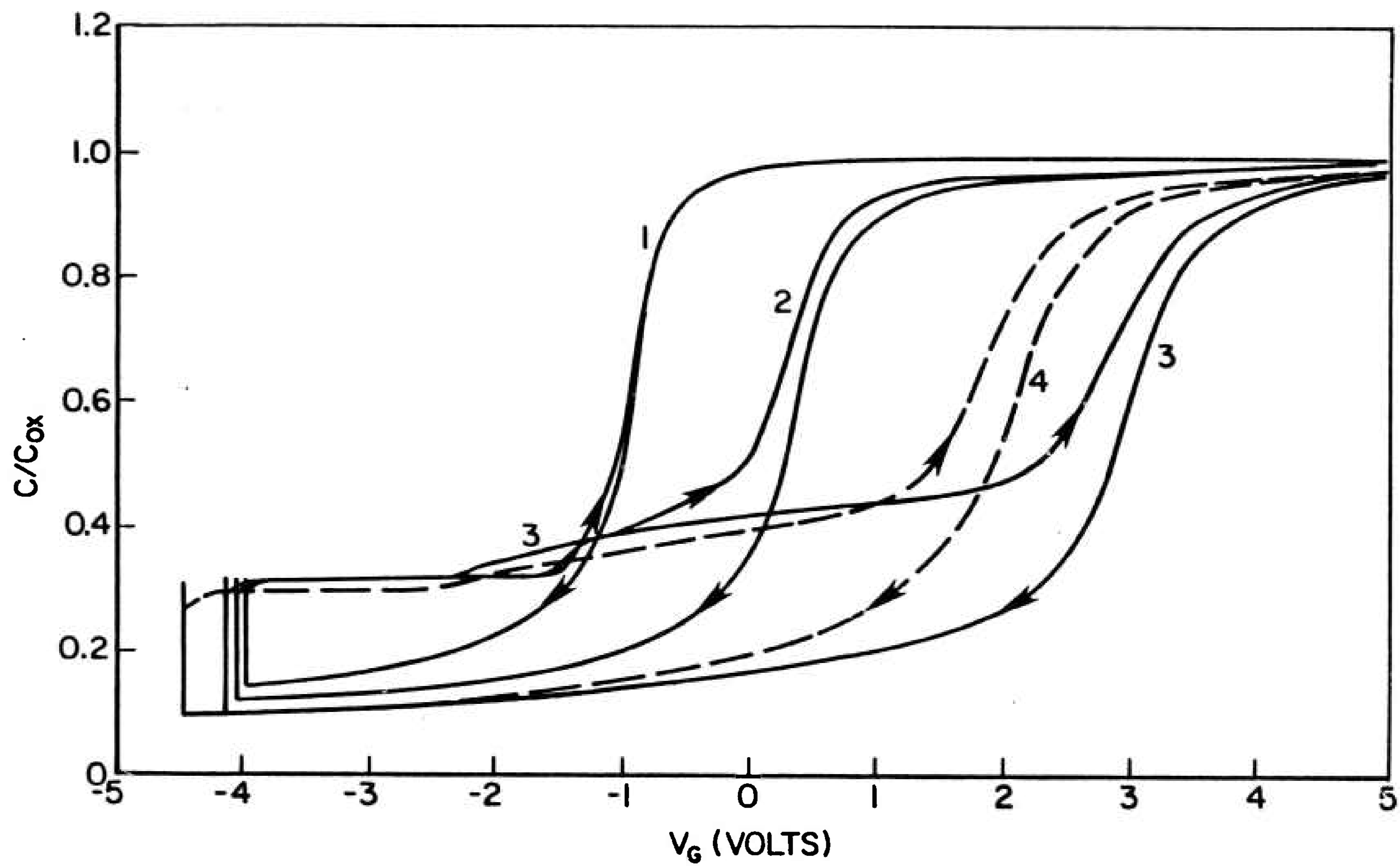

Fig. 2.1 C-V curves taken at 97°K, showing the effects of electron photoinjection from the substrate. Average field in the oxide was 1 MV/cm. The ramp rate was 1 V/sec. Curve 1: Fresh sample. Curve 2: After photoinjecting 0.054 C/cm^2. Curve 3: After photoinjecting 0.24 C/cm^2. Curve 4: After 4 days at room temperature.

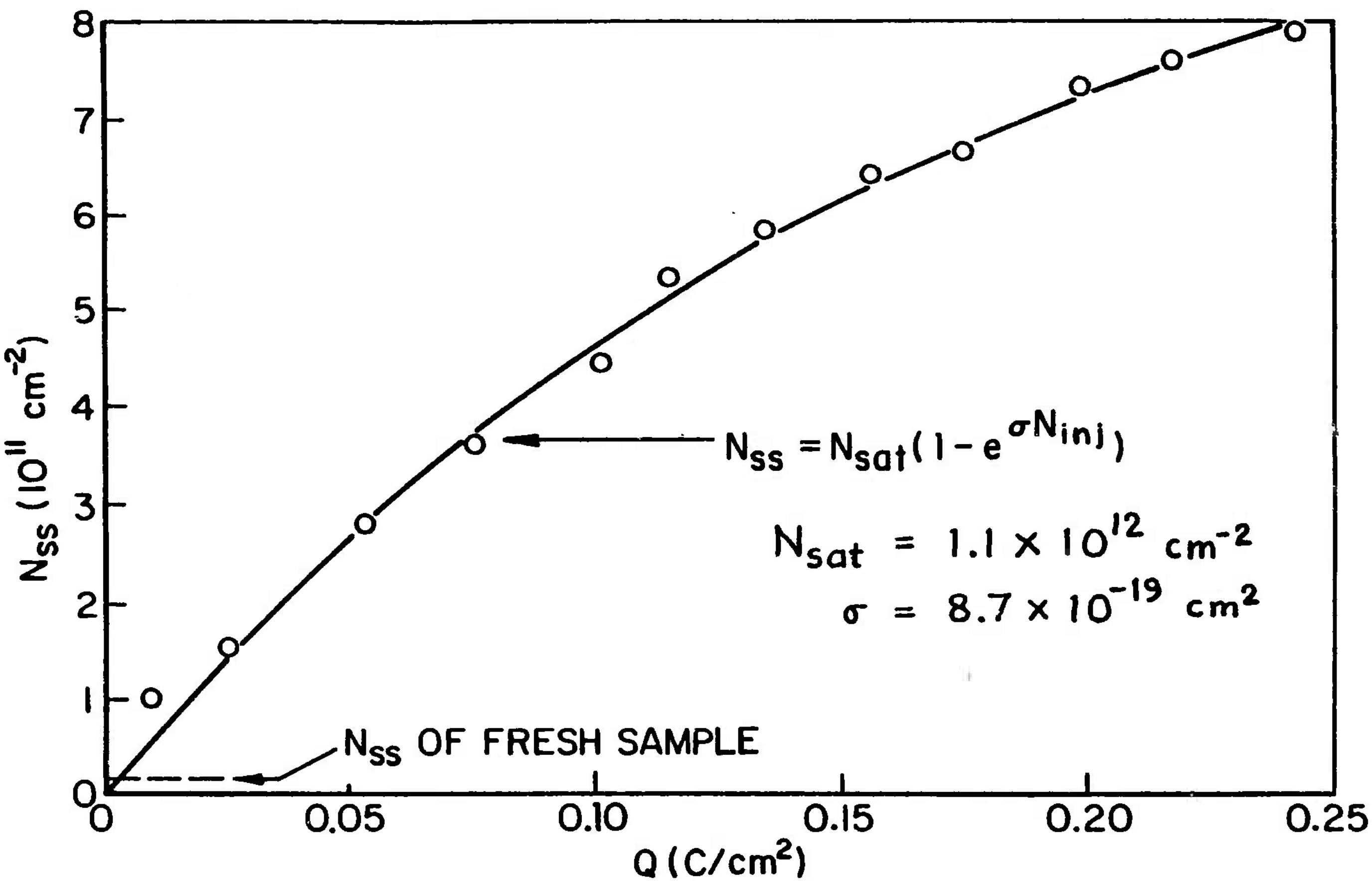

Fig. 2.2 The number of interface states generated as a function of the charge passed through the oxide at 97°K. Injection was from the substrate. Average field in the oxide was 1 MV/cm. The solid curve is an exponential (see text).

where N_{ss} is the areal density of generated interface states, N_{sat} is the saturated density of interface states, σ is the cross section for the creation of an interface state by an electron, and N_{inj} is the number of injected electrons per unit area. Using $N_{sat} = 1.1x10^{12}$ cm^{-2} and $\sigma = 8.7x10^{-19}$ cm^2 we obtain the solid curve in Fig. 2.2, which shows excellent agreement with the data. The initial slope here yields the product $\sigma N_{sat} = 9.6x10^{-7}$.

We also performed photoinjection experiments at 0°C. The initial interface-state generation was proportional to the amount of charge passed through the oxide. Typical numerical results were as follows: With a current density of 2.6 μA/cm^2 maintained for 5 hrs, the charge passed was 4.7 x 10^{-2} C/cm^2, and the interface-state density increased from 2 x 10^{10} cm^{-2}. The initial generation rate yielded the product $\sigma N_{sat} = 2.1 \times 10^{-6}$.

With negative bias applied to the Al field plate, electrons were photoinjected from the field plate into the insulator. With the smaller photoinjection barrier height, the electron current was larger than with positive field-plate bias. A typical result was as follows: At 97°K, with a current of 4.4 μA/cm^2 maintained for 2 hrs, the charge passed was $3x10^{-2}$ C/cm^2, and the interface-state density increased from $2x10^{10}$ cm^{-2} to $3.0x10^{11} cm^{-2}$. The initial generation yielded the product $\sigma N_{sat} = 1.5x10^{-6}$.

2.4. Annealing Properties of the Interface States

The interface states generated at either liquid-nitrogen temperature or at 0°C with either polarity of bias showed partial annealing at room temperature over long periods of time. Curve 4 of Fig. 2.1 was taken at 97°K after the sample had been kept at room temperature for 4 days. The C-V curves have shifted to the left and the interface density has decreased to $6.2x10^{11}$ cm^{-2}. Typically, the interface-state density decreased about 20% in a few days and about 40% in 5 months.

At higher temperatures, the generated states can be almost entirely annealed out. In preparation for an annealing experiment, a sample was photoinjected with 0.25 C/cm^2 with the field plate positive at liquid-nitrogen temperature, and showed an interface-state density of $7.9x10^{11}$ immediately after the photoinjection. With the sample open circuited and kept in the dark at room temperature for 5 months, the interface-state density was reduced to 4.7×10^{11} cm^{-2}. A set of isochronal anneals, of 15 min duration each, were then performed, with the results shown in Fig. 3.3. The interface-state densities plotted in that figure were, for the sake of consistency, obtained by cooling to liquid-nitrogen temperature and using the Jenq technique. The results of these measurements were confirmed by use of high-frequency and quasi-static C-V curves taken at room temperature. The results of Fig. 2.3 show that annealing of the generated interface states is rapid at temperatures above 200°C.

We find that a residue of negative charge ($\sim10^{11}$ electrons/cm^2) remains trapped in the SiO_2 after annealing. Preliminary photocurrent-voltage[16,17] experiments indicate that the negative charge resides very close to the Si-SiO_2 interface. This result is similar to that obtained by Solomon[9] in Fowler-Nordheim tunneling experiments. The residual negative charge in our samples was stable in vacuum at 400°C.

2.5. Conclusions

We have made a quantitative study of the interface states generated by a photoinjected electron current in MOS devices. The production of interface states depends upon the total charge passed through the SiO_2 in a manner which suggests the interpretation that there are sites in the SiO_2 at or near the Si interface that can interact with (possibly capture) an electron to produce an interface state. We deduce a site density of about 10^{12} cm^{-2} and an interaction cross section of 10^{-18}-10^{-19} cm^2 at 90°K. The product of site density and cross section does not show a strong dependence on the temperature at which the photoinjection is conducted or on the direction of electron flow. The similarity between the density and cross section we measure and those observed for electron traps in SiO_2[7-9] indicate that they may be related and that these interface states may have contributed to the flat-band and threshold shifts observed by other authors.

We find that the electron-current-induced states anneal slightly at room temperature. After 6 months with the sample open circuited, however, more than 50% of the original interface states remain. At a temperature of 200°C the interface states anneal rapidly and they can be almost completely

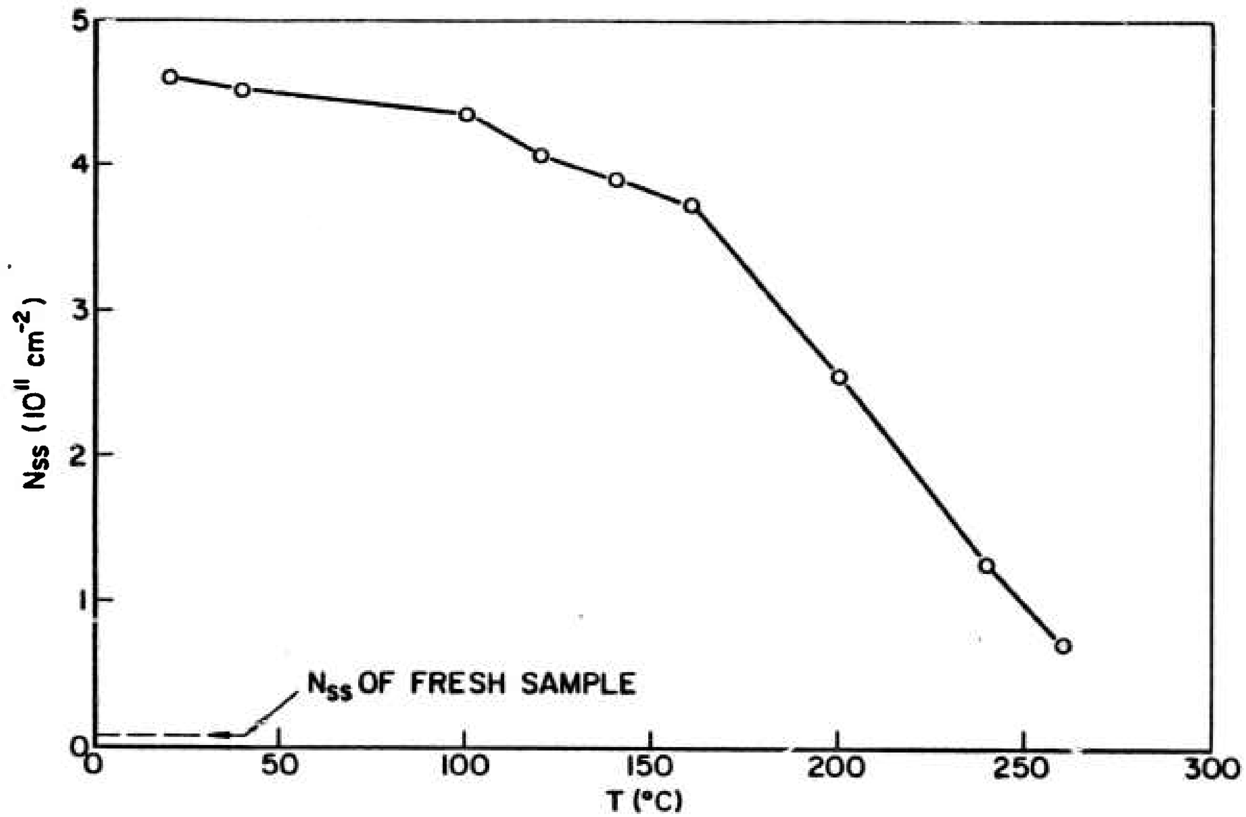

Fig. 2.3 Reduction of interface states by a set of isochronal anneals of 15 min duration each. A charge of 0.25 C/cm^2 had been photoinjected through the oxide at liquid-nitrogen temperature, and the sample had been kept at room temperature for 5 months prior to the annealing treatment.

eliminated at 300°C. After annealing, a residue of negative charge remains trapped near the Si-SiO_2 interface similar to that observed in Fowler-Nordheim tunneling experiments.[9]

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3. GENERATION OF INTERFACE STATES IN THE Si-SiO_2 SYSTEM DURING FOWLER-NORDHEIM TUNNELING OF ELECTRONS

(Chin-Jih Han collaborating)

3.1. Introduction

An important class of electrically erasable nonvolatile memory uses Fowler-Nordheim tunneling of electrons from silicon into a layer of SiO_2 to charge or discharge a floating gate and thus change the memory state of the cell.[1] Fowler-Nordheim tunneling is of interest for other reasons, also; for example, such tunneling is the first event in the sequence that leads to the dielectric breakdown of thermally grown SiO_2.[2,3] Lenzingler and Snow[4] and Osburn and Weitzman[5] observed that a greater voltage is required across an MOS structure to produce a given value of tunneling current as time goes on, and they conjectured that this might be due to electron trapping in the oxide. Solomon[6] investigated the electron trapping that accompanies Fowler-Nordheim tunneling and concluded that electrons are trapped about 10Å from the interface. He also noted that large numbers of interface states are formed and he had to anneal these away before measurement of the trapped charge could be accomplished. Since 10Å is within easy tunneling distance, the energy level of any such trapped charge would have to be below the valence-band edge of the silicon. The difference between such traps and so-called "interface states" is that the energy levels of the interface states are located in the forbidden gap of the semiconductor, and the states can therefore exchange charge with the semiconductor, depending on the position of the Fermi level at the interface. Tunneling requires the structure to be biased so as to bring electrons to the interface; therefore interface states would capture electrons and, if acceptor-like (negative when occupied), would have the same effect on the injected current as would "permanently" trapped electrons. These observations raise the question of whether the results observed by Lenzingler and Snow,[4] Osburn and Weitzman,[5] and Solomon[6] might have been caused at least partially by newly generated interface states instead of by electrons trapped in pre-existing sites. In this chapter we present the results of a study of the generation of interface states in the Si-SiO_2 system during Fowler-Nordheim tunneling.

3.2. Sample Preparation and Experimental Procedures

The samples used in these experiments were prepared by the Texas Instruments Corporation. The n-type silicon substrate was doped with phosphorus to 5-6 ohm-cm. The oxide on the substrate was grown at 1000°C with dry oxygen. The thickness of the oxide, as calculated from the oxide capacitance and the area of the field plate was 534Å ± 30Å. The field plates were of vacuum-deposited aluminum 1000Å thick and 0.0363 cm in diameter. The back of the wafer was etched and plated with aluminum to form an ohmic contact. After fabrication, the wafer was annealed at 450°C for 30 minutes in flowing hydrogen.

The high-field stressing was performed at room temperature with the field plate positive in polarity to induce Fowler-Nordheim tunneling of electrons from the Si substrate into the SiO_2. The current was recorded continuously while the stress was applied. Because of the initial transient caused by the switching-on of the power supply, current measurements were taken only after the power supply had been turned on for 2 minutes. Interface-state densities were determined from C-V measurements taken both at room temperature and at liquid-nitrogen temperature (the latter measurements were taken in order to use the Jenq low-temperature method,[7] which will be described briefly in the next paragraph). When making measurements at liquid-nitrogen temperature, the sample chamber was held to a rough (10 milliTorr) vacuum to reduce difficulties with moisture.

The Jenq C-V technique[7] of measuring interface states uses two voltage sweeps in opposite directions at low (e.g., liquid-nitrogen) temperature so that charge carriers are frozen into the interface states except for those states so near the band edges that emission can take place even at lowered temperature (∿0.2 eV at 90°K).[7] Thus, the measurement includes the interface states within the ∿0.7 eV central region of the silicon band gap. The first voltage sweep was started in the accumulation region and was ramped down at 1 V/sec until the sample was in deep depletion. The sample was then briefly exposed to light from a high-intensity lamp to generate minority carriers, which brought the sample into inversion. The light was turned off, and the voltage was ramped back toward accumulation. During the first sweep, majority carriers are frozen into the states, while during the second sweep, minority carriers are frozen into the states. The resulting difference in charge at the interface causes the two curves to have parallel sections which differ by a translation, ΔV, along the voltage axis. This can be seen in the pair of curves labeled (1) in Fig. 3.1, where section A of the downsweep is ΔV volts to the right of section B of the upsweep. The number of interface states per unit area is given by

$$N_s = \frac{C_{ox}}{e} \Delta V \tag{3.1}$$

where C_{ox} is the oxide capacitance per unit area and e is the magnitude of the electronic charge.[7]

3.3. Generation of Interface States

A typical set of C-V curves is shown in Fig. 3.1. Curve 1 is the room-temperature high-frequency (1 MHz) C-V curve before the high-field stress. The sample was then stressed, field plate positive, to an average oxide field of 7.0 MV/cm for 4 hrs. Curve 2 shows the room-temperature C-V curve after stressing. The stretch-out shows the presence of fast interface states, and the hysteresis can be attributed to slow interface states, as will be discussed later. Figure 3 shows deep-depletion (downsweep) and post-illumination (upsweep) C-V curves taken at 97°K. The parallel portions A and B show $\Delta V = 4.8$ V. Use of Eq. 3.1 provides the result $N_s = 2.0 \times 10^{12}$ cm^{-2} in approximately the central 0.7 eV region of the Si bandgap. This is to be contrasted with the result obtained before stressing. The pre-stress low-temperature C-V curve (not shown in Fig. 3.1) was quite close to Curve 1 and showed a value of ΔV smaller than 0.1 V (the minimum measurable amount), which indicated an initial interface-state density less than 4×10^{-10} cm^{-2}. The results of a series of measurements, each using a fresh sample, are shown in Fig. 3.2 for average fields ranging from 6.5 to 7.3 MV/cm (field plate positive). The

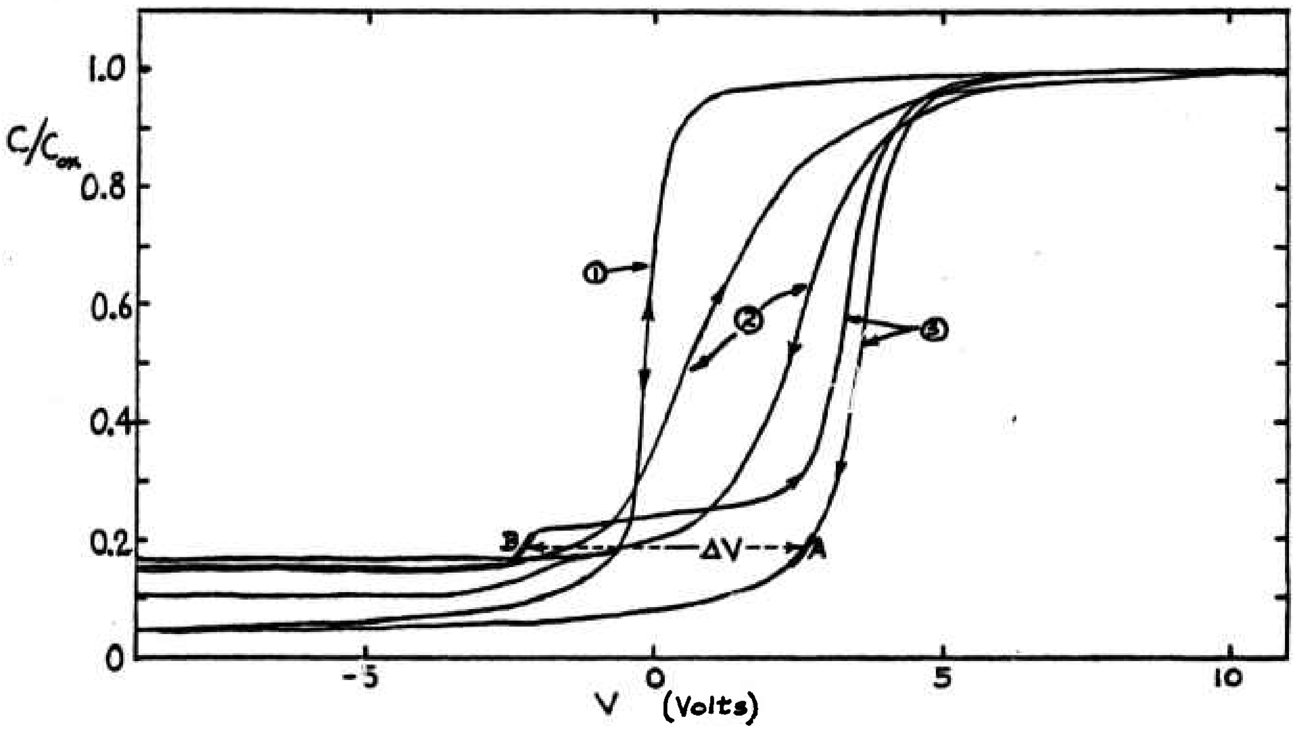

Fig. 3.1. High-frequency (1 MHz) C-V curves of a sample stressed at room temperature at an average field of 7.0 MV/cm (field plate positive) for 4 hrs. Curve 1: Room-temperature C-V curve of the fresh sample. Curve 2: Room temperature C-V curve after stress. Curve 3: C-V curves taken at 97°K (see text) after stress. The low-temperature curves for the fresh sample were quite close to Curve 1 and showed an interface-state density smaller than 4×10^{10} cm^{-2}.

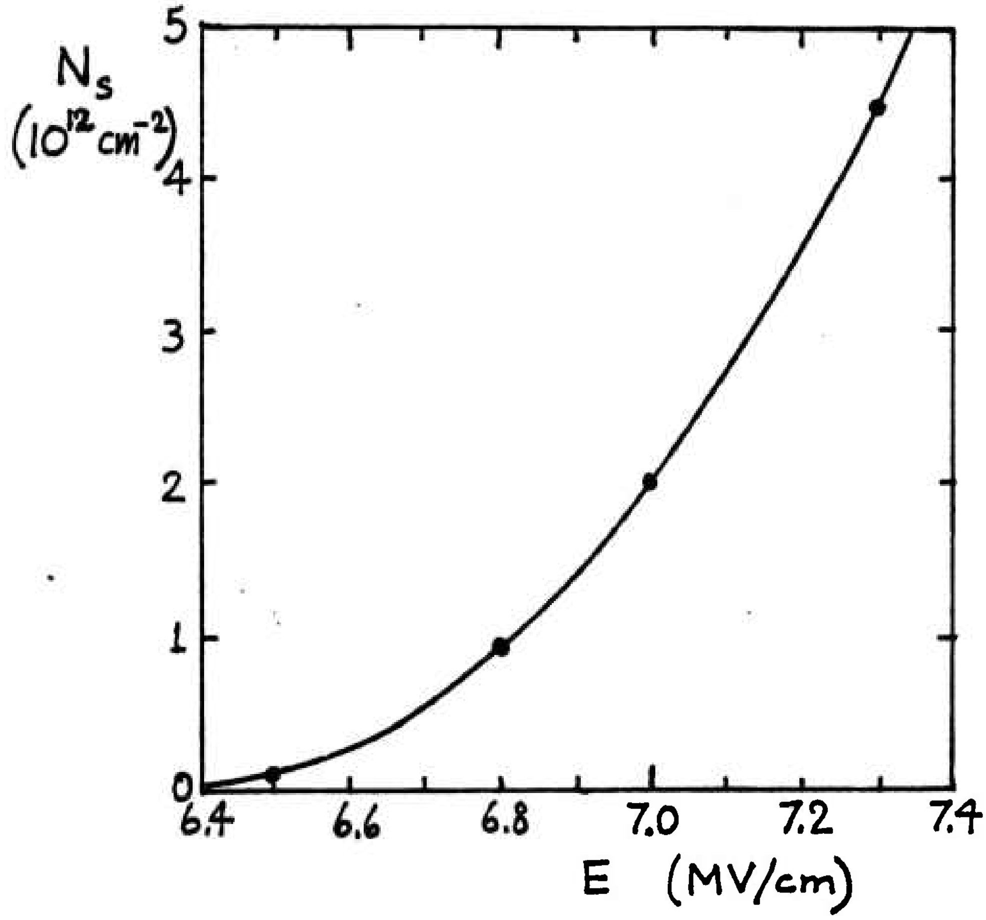

Fig. 3.2. Density of generated interface states, as measured by the Jenq low-temperature technique, vs. average electric field (field plate positive) applied for 4 hrs at room temperature. A fresh sample was used for each point.

stress was applied for 4 hours for each measurement. It should be observed that the electric flux from 4.5×10^{12} electrons/cm^2 is sufficient to produce an electric field of 2.1 MV/cm in the oxide.

A striking feature of the room-temperature post-stress C-V curves is the hysteresis, as is shown by Curve 2 of Fig. 3.1. Solomon[6] showed a similar hysteresis in Curve 2 of his Fig. 9. The direction of the hysteresis is opposite to what would be caused by ionic motion. For example, if the oxide contained mobile positive ions, a positive field-plate voltage would cause the ions to drift toward the $Si-SiO_2$ interface, where they would cause the flatband voltage to become more negative. Mobile negative ions would cause the same shift, whereas the opposite of this is seen. We believe that the hysteresis is caused by "slow" interface states which are generated along with the "fast" states that cause Curve 2 of Fig. 3.1 to be stretched out with respect to Curve 1. Either the slow states are of unbelievably small cross section (say, $\sim 10^{-25}$ cm^2) or, as seems more likely, they are simply located in the oxide further from the interface, thus reducing the tunneling probability and causing the same effect as a small cross section.[8,9] In an attempt to bring the slow states into thermal equilibrium during the sweep, we slowed the ramp rate; however, only minor differences were found with ramp rates in the range of 4 mV/sec to 1 V/sec. With a slow sweep, states further from the interface could fill, but they would have sufficient time to empty during the sweep back. We believe, therefore, that states are generated not only at the interface during Fowler-Nordheim tunneling, but also deeper within the oxide. The width of the hysteresis loop was 4.4 V for a stress field of 7.3 MV/cm applied for 4 hrs. This hysteresis indicates the rather large difference of 1.8×10^{12} charges/cm^2 between the up and down sweeps.

In order to check the interface-state generation measured by Jenq's low-temperature method and shown in Fig. 3.2, we analyzed the post-stress room-temperature C-V curves by Terman's method.[10] For example, starting with Curve 2 of Fig. 3.1, we averaged the voltages for the up- and down-sweeps, and used this single curve in the calculation. The result for the specimen stressed at 7.0 MV/cm is shown in Fig. 3.3, where the density of interface states in cm^{-2} eV^{-1} is plotted against surface potential. The integral of this from midgap to 0.2 eV below ε_c indicates a number of interface states in this energy range equal to 8.0×10^{11} cm^{-2}. If we simply multiply this by 2 to take account of the lower half of the band-gap, we obtain $N_s = 1.6 \times 10^{12}$ cm^{-2} for the number of states in the expected measurement range of the Jenq technique. This compares reasonably well with the value $N_s = 2.0 \times 10^{12}$ cm^{-2} measured by the Jenq method and plotted at 7.0 MV/cm in Fig. 3.2.

Since the current was monitored during the experiments, the total charge passed through the interface could be obtained by integrating the observed current over time. An interesting result is obtained when the number of interface states generated in 4 hrs. is plotted against the total charge passed. This is shown in Fig. 3.4, where it is seen that the data points lie reasonably well on a straight line through the origin. The slope of this curve, which was obtained by a least-squares fit, corresponds to 3.68×10^{-5} states formed per electron passed through. This is an order of magnitude larger than the value $\sigma N_{sat} = 2.1 \times 10^{-6}$ quoted in Sec. 2.3 of this report for electrons photoinjected at 0°C at a field of 1 MV/cm. Furthermore, our data show no saturation up to $N_s = 4.4 \times 10^{12}$ cm^{-2}. Such differences might be caused by a field effect or by differences in oxide growth and processing, but the connection, if any, between the results given in Ch. 2 and those presented here for Fowler-Nordheim tunneling has yet to be proved.

3.4. Location of the Centroid of the Negative Charge

As the Fowler-Nordheim tunneling of electrons progresses at a given value of average applied field, the current continuously decreases in the manner shown by the discrete data points in Fig. 3.5. (The solid curves were calculated from a model which will be discussed in the next section.) The reduction in current is considerable at the higher fields; for example, at an average field of 7.3 MV/cm, the current decreased in 4 hrs. to 15% of its initial value. This is the result of negative charging in the oxide,

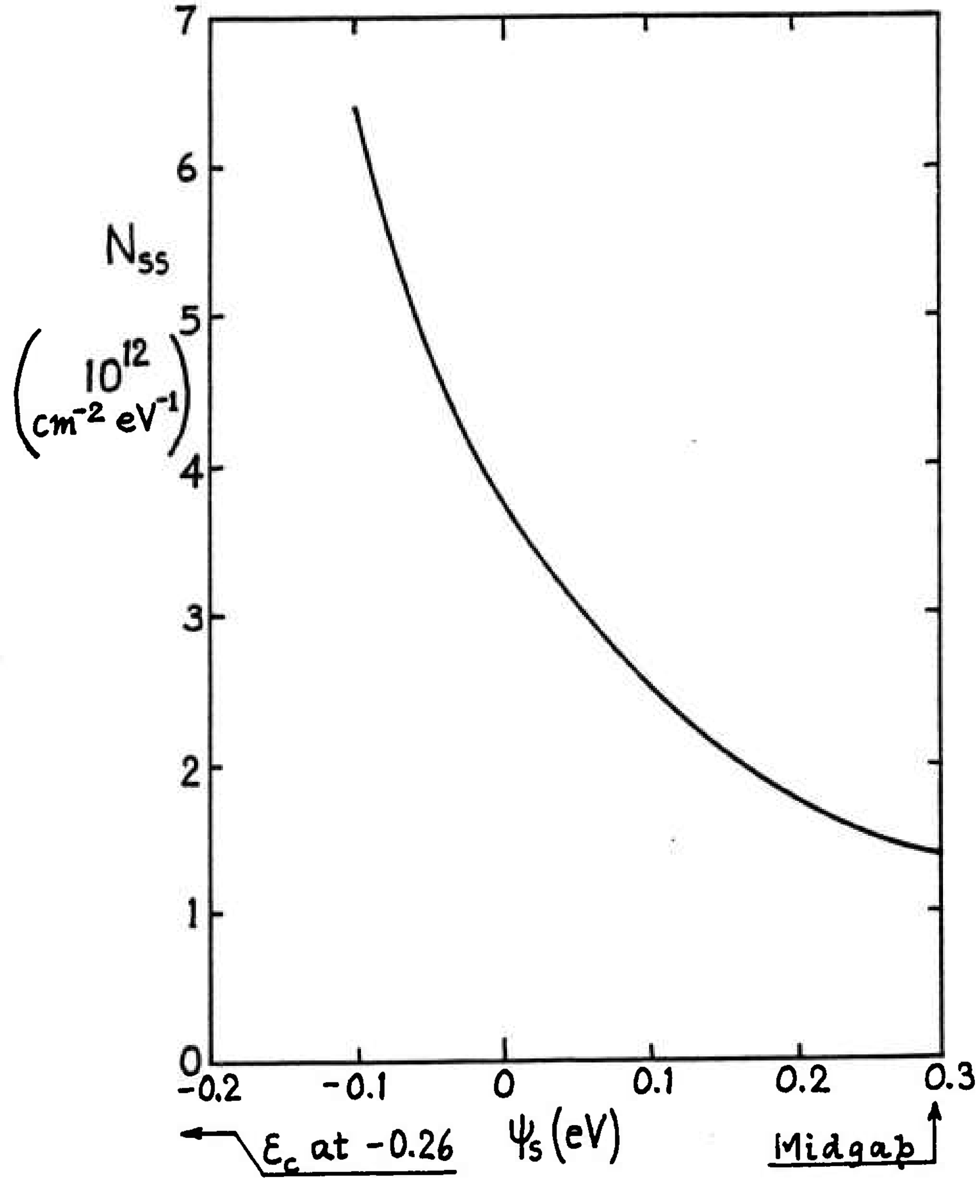

Fig. 3.3. Density of interface states, as determined by Terman's method, vs. surface potential, after 4 hrs stress at 7.0 MV/cm.

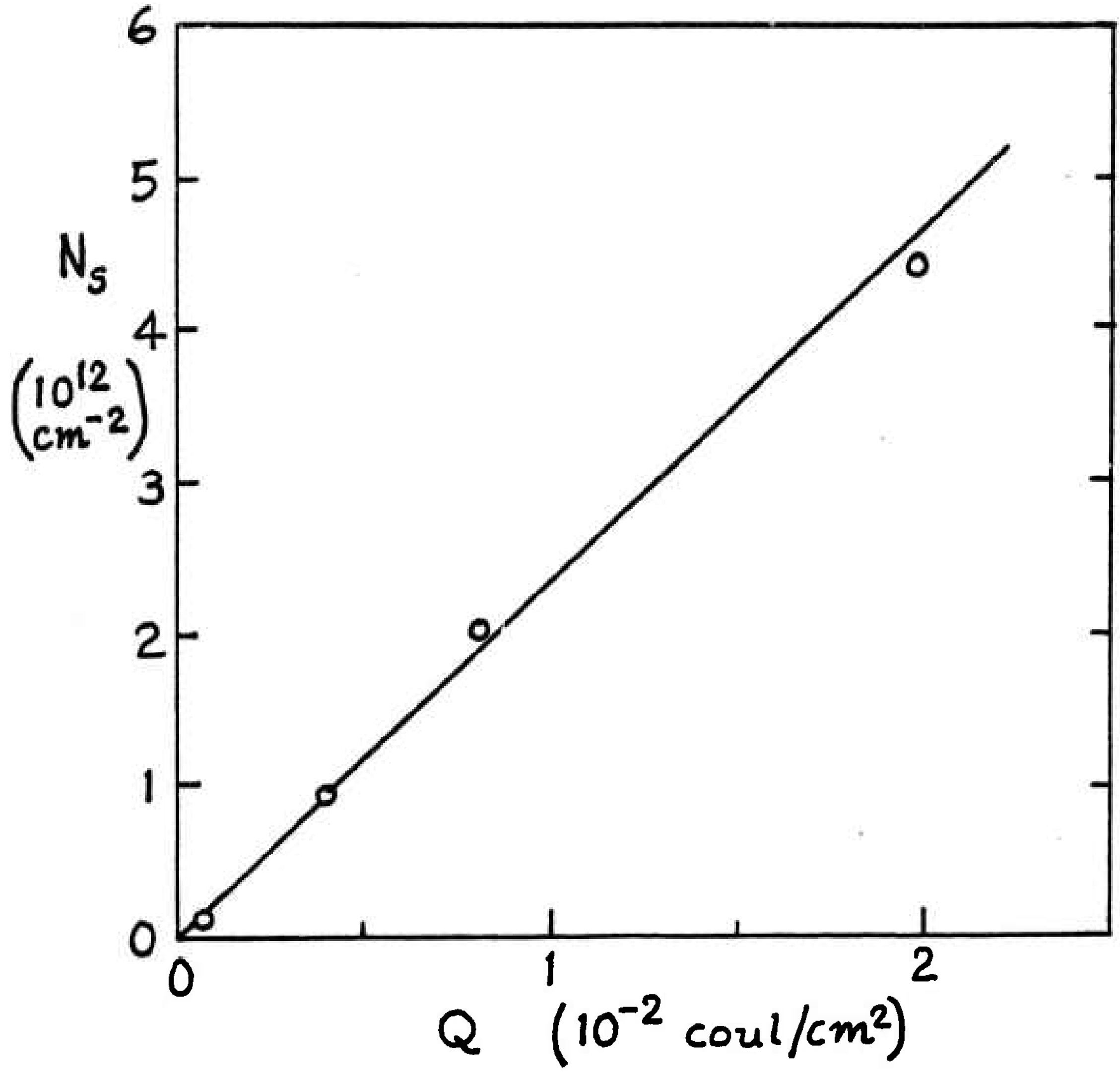

Fig. 3.4. The density of generated interface states, as measured by the Jenq low-temperature technique, plotted against the total amount of charge passed through the interface. The points correspond to those shown in Fig. 3.2, which we obtained by stressing fresh samples for 4 hrs each at fields of 6.5, 6.8, 7.0 and 7.3 MV/cm, respectively, at room temperature. The straight line was obtained from a least-squares fit, and has a slope of 2.30×10^{14} states/coulomb or 3.68×10^{-5} states/electron.

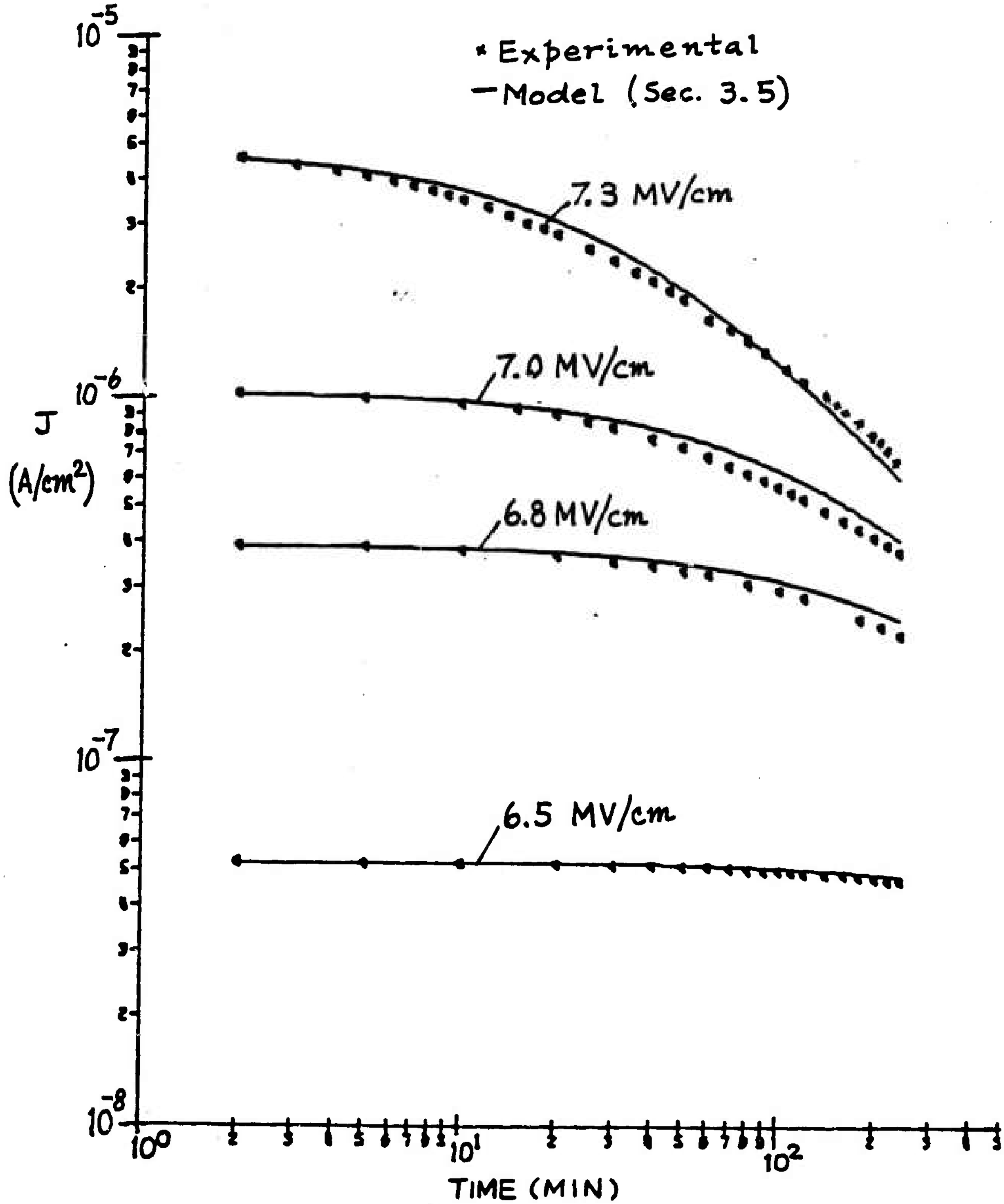

Fig. 3.5. Current density vs. time at constant average values of electric field.

which raises the Fowler-Nordheim barrier in the manner discussed by Solomon.[6] At fields above 7.5 MV/cm, the current tended to become unstable and eventually increased, presumably because of impact ionization within the SiO_2 followed by hole trapping near the Si-SiO_2 interface.[2,3]

For a given voltage across the oxide, a sheet of charge that is located exactly at the Si-SiO_2 interface cannot alter the field in the oxide, for this charge will be compensated by an opposite charge supplied by the semiconductor. The negative charge that raises the Fowler-Nordheim barrier must, therefore, be located in the interior of the oxide. In this section we present an estimate of the position of the centroid of the negative charge. Schottky image-force barrier lowering will be neglected, and we shall assume that we can neglect the discrete character of the charges even though they may be located quite close to the interface.

The basic model for this calculation is illustrated in Fig. 3.6. The dashed curve marked ε_o shows the location of the conduction band edge if no charges are in the oxide. The charges are represented by a sheet of charge located at the position of the centroid, a distance d away from the interface. The extension of the band edge near the Si-SiO_2 interface intercepts the SiO_2-metal interface ΔV volts above the bias voltage, whereas the actual band edge extends to the bias voltage level. Insofar as the electric field at the Si-SiO_2 interface is concerned, the effective voltage is $V-\Delta V$.

The equations for the conduction band edges may be written as follows, taking $\varepsilon_1 = 0$ at $x = 0$:

$$\varepsilon_1 = -e\left(\frac{V-\Delta V}{L} x \right)$$

and (3.2)

$$\varepsilon_2 = e\left(\Delta\phi - \frac{V+\Delta\phi}{L} x\right) \quad ,$$

where L is the width of the oxide, V is the bias voltage, and $\Delta\phi$ is the imaginary increase in barrier height if one extends ε_2. Solving for the

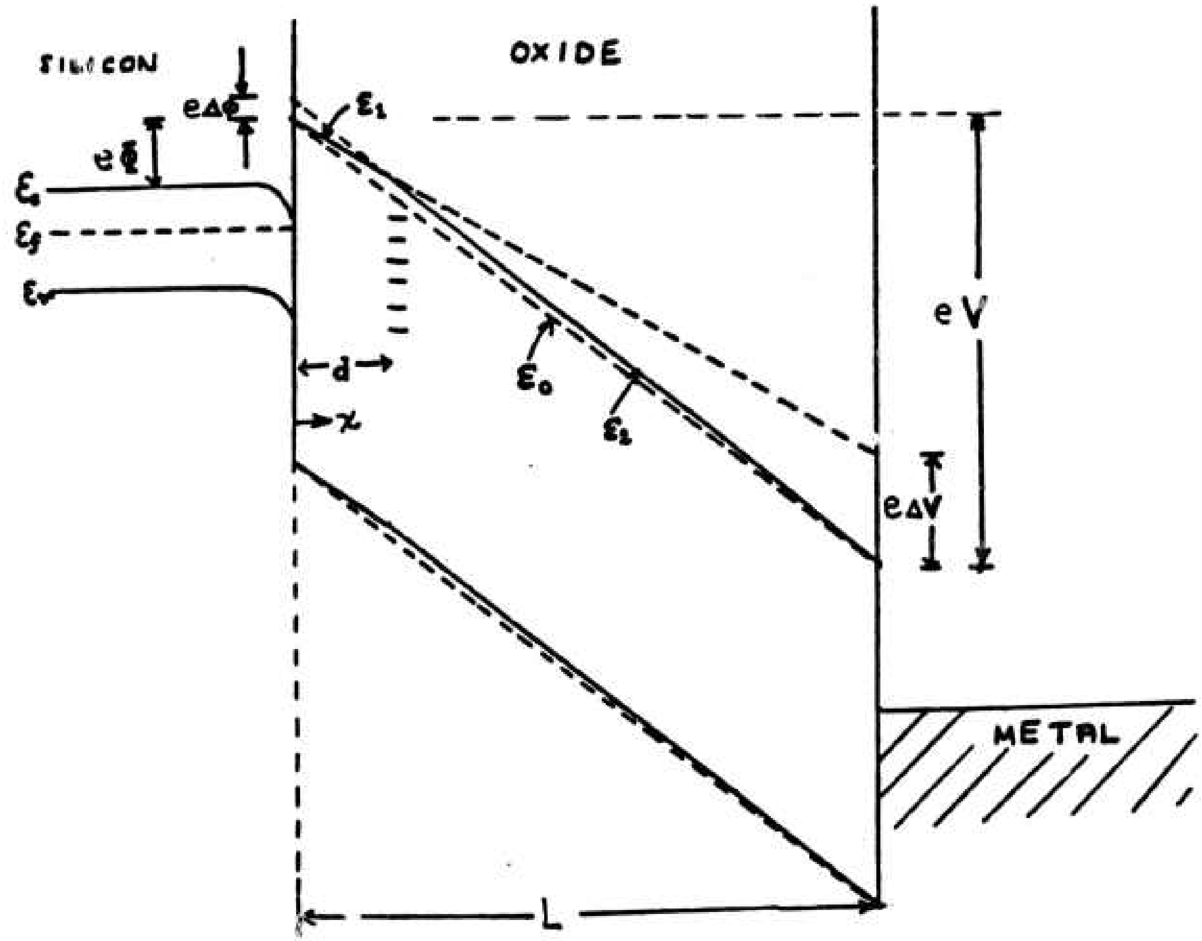

Fig. 3.6. Effect of a negative charge having its centroid located a distance d from the Si-SiO_2 interface.

common point of the two curves, we obtain

$$\Delta\phi = \frac{\Delta V}{L} \; d \quad . \tag{3.3}$$

For the purpose of making calculations of Fowler-Nordheim tunneling, ε_2 and its extension is a good approximation for the shape of the band edge. The tunneling problem has already been solved for a triangular barrier having a uniform electric field $E = -(1/e)d\varepsilon/dx$. The electric-field dependence of current density for such a barrier is[12]

$$J = \frac{e^2E^2}{8\pi h\phi} \exp[-4(2m)^{1/2}(e\phi)^{3/2}/3\hbar eE] \tag{3.4}$$

where ϕ is in eV. Before charging, $J = J_o$ is given by Eq. (3.4) with $E = V/L$. For the current after charging, we replace ϕ by $\phi + \Delta\phi$ and, from Eq. (3.2), use $E = -(1/e)d\varepsilon_2/dx = (V + \Delta\phi)/L$. Then the ratio of current densities after and before charging is

$$\frac{J}{J_o} = \frac{(V+\Delta\phi)^2}{V^2(\phi+\Delta\phi)} \exp\left\{- \frac{4}{3} (2m)^{1/2} \frac{L}{\hbar e} \left[\frac{(e\phi+e\Delta\phi)^{3/2}}{V+\Delta\phi} - \frac{(e\phi)^{3/2}}{V}\right]\right\} \tag{3.5}$$

The exponential is much more important than the pre-exponential factor. Also, $\Delta\phi$ is much more important in $\phi+\Delta\phi$ than in $V+\Delta\phi$. Then, using the binomial expansion $(\phi+\Delta\phi)^{3/2} \approx \phi^{3/2} + 3\phi^{1/2}\,\Delta\phi/2$, we can write, approximately,

$$\frac{J}{J_o} = \exp[-2(2em)^{1/2} \, L\,\phi^{1/2} \, \Delta\phi/\hbar V] \tag{3.6}$$

Substituting for $\Delta\phi$ from Eq. (3.3) and solving for the position of the centroid, d, we obtain

$$d = \frac{\hbar V}{2(2em)^{1/2}\phi^{1/2}\Delta V} \; \ln(J_o/J) \tag{3.7}$$

A knowledge of J_o, J, and the voltage shift of the C-V curve will yield the value of d. For example, for E = 7.0 MV/cm we obtain from Fig. 3.4: $J_o = 1.0 \times 10^{-6}$ A/cm^2 and, at the end of 4 hrs, $J = 3.6 \times 10^{-7}$ A/cm^2. In Fig. 3.1, we need to try to estimate the voltage shift, ΔV, between Curve 2 and Curve 1 in the heavy accumulation region corresponding to an applied voltage of $(5.34 \times 10^{-6}$ cm$) \times (7.0 \times 10^{6}$ V/cm$) =$ 37 V, for it was at this bias that the Fowler-Nordheim tunneling occurred. We cannot simply take ΔV at the flatband point, for this would ignore all negative charge in interface states above the flatband Fermi-level position. From Fig. 3.1, as accumulation is approached, Curve 2 is no less than 4 volts to the right of Curve 1; therefore we can only say that $\Delta V \geq 4$ V. Thus, Eq. (3.7) can only give an upper bound on the value of d. The results obtained by this method, using $m = 0.43\ m_o$ (Ref. 12) and $\phi = 3.1$ eV, are shown in Table 3.1.

Table 3.1

Calculated Positions of Centroids of Negative Charge

E(MV/cm)	J(4hrs)/J_o	d ≤ (Å)
6.5	0.89	11.5
6.8	0.56	9.0
7.0	0.36	7.5
7.3	0.15	6.5

The results shown in Table 3.1 are not much different from the 5-10Å estimate obtained by Solomon[6] for the fixed charge that remained after the interface states were annealed away. The difference here is that we are including the negative charge in interface states, and, in fact, from the appearance of Fig. 3.1, where the stretch-out is at least as large as the translation, it would appear that interface states may be more important than the fixed charge.

3.5. Model for Current Reduction

One may try to use the observation that the density of interface states is proportional to the total charge flow and try to predict the current behavior from it. In the last section, the location of the centroid of the interface states was calculated to be about 7Å away from the interface. The following model uses this result in a modified Fowler-Nordheim tunneling equation to calculate the current behavior.

Our model is basically that shown in Fig. 3.6, in which a sheet of charge with density σ is located at a distance d from the Si-SiO_2 interface. The value of d is taken to be fixed in the calculation. The charge density σ is taken to be proportional to $\int J\,dt$. The electric field between the field plate and the sheet charge is E_2. The field between the charge and the Si-SiO_2 interface, E_1, is smaller than E_2 by σ/ε, where ε is the dielectric constant of the oxide.

Neglecting work-function differences and the voltage drop in the semiconductor, we can write the following equation for the bias voltage V:

$$V = E_2(L - d) + (E_2 - \frac{\sigma}{\varepsilon})\, d \quad .$$

Rearranging terms, we have:

$$E_2 L = V + \frac{\sigma}{\varepsilon}\, d \quad . \tag{3.8}$$

The second term on the right side of the equation can be thought of as an imaginary bias voltage one must add on if the electric field is to be E_2. This term is the same imaginary voltage that was denoted by $\Delta\phi$ in Fig. 3.6. The field E_2 is a function of time through σ, and σ is proportional to the total charge that has passed through the interface. As in Sec. 3.4, the tunneling barrier for electrons will be approximated by E_2 of Fig. 3.5, and we can then use Eq. (3.4) with ϕ replaced by $\phi' = \phi + \Delta\phi = \phi + \sigma d/\varepsilon$. Since σ and therefore E_2 are both functions of time, the tunneling equation is an integral equation and may be evaluated numerically. First the derivative of J is taken. The pre-exponential factor varies slowly compared to the exponential and is treated as a constant in the differentiation. The time derivative of J is

$$\frac{dJ}{dt} = - \frac{e^4(2m)^{1/2}}{3h^2\varepsilon} \; SdEJ(t) \left[\frac{3}{2}\,(e\phi')^{-1/2} - \frac{(e\phi')^{1/2}}{eEL}\right] \exp\left[-\frac{4}{3}\,\frac{(2m)^{1/2}(e\phi')^{3/2}}{\hbar eE}\right] \qquad (3.9)$$

where S is the slope of the relationship N_s vs. Q. From Fig. 3.4, S = 2.30×10^{14} states/coulomb. The results of the numerical integration are plotted as the solid lines in Fig. 3.5. These curves not only exhibit the same shape as the experimental results but also lie reasonably close to the experimental values.

3.6. Summary and Discussion

The Fowler-Nordheim tunneling of electrons from the Si into the SiO_2 of an MOS structure is found to be accompanied by the generation of interface states, as is shown by measurements made by the Jenq low-temperature C-V technique and by calculations made from the room-temperature C-V curves by Terman's method. In our dry-oxide samples which had been annealed in hydrogen, the rate of interface-state generation increased rapidly as the field was increased in the range 6.5 - 7.3 MV/cm. The number of interface states generated in 4 hrs was proportional to the charge passed through the interface, up to a field of 7.3 MV/cm, which produced 4.4×10^{12} interface states/cm^2. A least-squares straight-line fit to the data indicated a slope of 2.30×10^{14} states produced per coulomb of charge in the range 0 - 0.02 C/cm^2.

For constant average values of electric field below 7.5 MV/cm, the tunneling current continuously decreases in value as time goes on. (At fields above about 7.5 MV/cm, the current is unstable and eventually increases. This is caused by impact ionization followed by hole capture, a phenomenon that we are not concerned with here.[2,3]) The reduction of current is caused by a buildup of negative charge in the oxide. Under the assumption that most of this charge resides in the newly generated interface states, we estimated the position of the centroid of charge to be 6-12Å from the $Si-SiO_2$ interface. Based on this same model, we computed the time evolution of the tunneling current and found reasonable agreement with the experimental results.

As usual, it is not possible to distinguish the effect produced by acceptor-type interface states from those produced by a combination of donor-type states and a fixed negative charge. From an examination of both Solomon's results[6] and our own, we can offer some observations and opinions, however. Interface states are certainly generated during the tunneling, as is shown by the stretch-out of Curve 2 in Fig. 3.1 compared with Curve 1 and also by the translation ΔV between sections A and B of the low-temperature curves. Terman's method applied to Curve 2 and Jenq's formula applied to Curve 3 produce substantially identical results. As accumulation is approached, Curve 2 goes farther and farther to the right of Curve 1, indicating an increased capture of electrons by interface states as the electron concentration at the interface is increased. The amount by which Curve 2 is to the right of Curve 1 in heavy accumulation cannot be measured, but it is surely greater than 4 volts. If we were to assume that the negative charge which causes the reduction in current is fixed in the oxide, we would have to say that the fixed charge caused a flatband shift greater than +4 volts and that the interface states were of the donor type, i.e., that the states were neutral in the presence of a heavy accumulation of electrons. Solomon[6] found a relatively smaller flatband shift after a rather gentle annealing of the interface states. The appearance of all of our C-V curves, of which Fig. 3.1 is an example, suggests the following interpretation: The passage of electrons from the Si into and through the SiO_2 causes the formation of charge-trapping sites in the amorphous transition region between the Si and the bulk SiO_2, and perhaps in the SiO_2 beyond the transition region. The energy levels of the trapping sites are spread over a spectrum because of the amorphous character of the structure and the resulting differences in angle and distance to neighboring atoms. In the presence of a concentration of free electrons at the interface, some of the trapping sites near the interface gain one electron each and become negative. These are the acceptor-type states. In the presence of holes at the interface, some of the sites - the donor-like states - lose an electron and become positive. Still other sites are able to keep an extra electron after they gain it, even in the presence of holes. This may occur either because the original energy level was below the top of the Si valence band, or because relaxation of the ions in the neighborhood caused the occupied level to fall low enough in energy. The states that can cyclically exchange charge with the substrate are, by definition, the "interface states," and the sites that retain electrons are "electron traps." Sites that are not located at the interface but are within tunneling distance can exchange charge with the substrate, but the tunneling probability goes down rapidly with distance, giving an effect that is much the same as a very small cross section.[8,9] The shape of the low-temperature curves, such as Curve 3 in Fig. 3.1, can be explained by assuming that there is a comparatively modest amount of fixed negative charge and that either the donor-type and acceptor-type interface states are present in about equal numbers or else the sites are amphoteric in character; i.e., the same site can either lose an electron and become positive or gain an extra electron and become negative. With this interpretation, we would estimate in Fig. 3.1 that the fixed negative charge caused a flatband shift of slightly less than one volt to the right, this being the midpoint of the horizontal line marked "ΔV", and we would suppose that sections A and B fall 2.4 volts to the right and left, respectively, of the midpoint because of the acceptor/donor character of the states.

These studies are continuing.

3.7. References

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4. A STUDY OF RADIATION-INDUCED INTERFACE STATES IN MOS CAPACITORS

(J.K. Wu collaborating)

4.1 Introduction

Winokur et al[1,2] found that radiation-induced interface-state generation in the $Si-SiO_2$ system does not depend on the direct interaction of radiation with the $Si-SiO_2$ interface, but occurs after radiation-generated holes had time to reach the interface. McLean et al[3] found that at liquid nitrogen temperature the transport of holes from their point of generation to the interface is reasonably rapid under a 4-6 MV/cm electric field, but that the transport is very slow at smaller fields. Jenq,[4,5] investigating the generation of interface states by high-field stress, and Clement,[6] investigating interface-state generation after X-irradiation, found that the states were not generated as long as the sample was held at low temperature, but began to appear only as the sample was warmed. Genda Hu[7] studied the interface states that are associated with trapped holes, and found that by annihilating the holes with photoinjected holes immediately after X-irradiation at low temperature, the generation of interface states could be stopped. Jenq,[4,5] however, found what appeared to be a second species of interface state that is associated with the passage of electrons through the interface rather than with the presence of holes.

We have made a further study of the relationship between trapped holes near the interface and the generation of interface states. Also, we have tried to deduce the acceptor-like or donor-like character of the generated states.

4.2. Samples and Experimental Procedures

Our samples were MOS capacitors which were fabricated at Bell Laboratories by courtesy of E.N. Fuls. The substrates were n-type (100) Si of 5-10 Ω cm resistivity. The oxides were thermally grown in dry oxygen with 3% HCL to a thickness of 1190Å. The field plates were of

Al and were about 120Å in thickness. This was thin enough to allow us to photoinject electrons. The devices were sintered in H_2 at 450°C for 30 min after Al evaporation.

In these experiments we used the Low Temperature C-V Displacement (LTD) method proposed by Jenq[8] to measure the density of interface states. Two C-V curves are taken at 85°K, one with majority carriers (electrons) frozen into the interface states and the other with minority carriers (holes) frozen into the states. The two C-V curves have parallel portions that differ by a translation along the voltage axis owing to the different amounts of charge at the interface. The number of interface states per unit area is given by $N_s = C_{os}\,\Delta V/e$, where C_{ox} is the insulator capacitance per unit area, ΔV is the translation between the two curves, and e is the magnitude of the electronic charge. The method includes all interface states except those so close to a band edge that they can emit their charge carriers during the short time required to record a C-V curve. Measurements requiring a few seconds allow states within ∿0.2 eV of a band edge to emit their carriers at 85°K; thus, at this temperature, the Jenq technique includes those interface states lying within approximately the central 0.7 eV portion of the silicon bandgap.

Each MOS capacitor was first cooled to 85°K, and the initial C-V curve was taken. Following this, the sample was exposed to soft x-rays in the manner previously described by J.J. Clement.[6,9] A 12V gate-positive bias (∿1 MV/cm) was applied across to the MOS capacitor, and the typical irradiation time was 6 minutes. Soft x-rays generate electron-hole pairs in the oxide; the electrons are rapidly swept out by the bias field, the holes are essentially immobile at 85°K and 1 MV/cm and are trapped throughout the oxide near the point of their creation.[3] There is a negative flat-band voltage shift owing to the positive space-charge build-up in the oxide. After recording the magnitude of the shift, a 60V gate-positive bias (∿5 MV/cm) was applied to the sample to cause the holes to drift as near the interface as possible. The sample was then illuminated by ultraviolet light having a photon energy of about 5 eV which resulted in the internal photoemission of electrons from the silicon substrate into the oxide, where some of the electrons recombined with holes. The electric field applied to the sample was 1 MV/cm, gate positive.

4.3 Results

We first tested the concept that interface states will not develop if holes trapped at the interface at liquid nitrogen temperature are annihilated before the sample is warmed. For this purpose we utilized photoinjected electrons. The sample was first cooled to 85°K and exposed to soft x-rays for 6 minutes to generate hole-electron pairs in the oxide. A moderate gate-positive bias of 12 volts (∿1 MV/cm) was applied during the irradiation to drift the electrons out of the oxide. This field is not sufficient to move the holes appreciably.[3] A 60-volt (∿5 MV/cm) gate-positive bias was then applied to the sample for 9 hours. The 5 MV/cm stress field is not high enough to create electron-hole pairs through impact ionization, but is sufficient to transport most of the holes to the interface,[3] where some of them are trapped. We found that the C-V curve first shifted in the negative direction as the centroid of the holes moved toward the Si-SiO_2 interface, and then shifted back as some of the holes were lost by passing through the interface into the silicon. The position of the C-V curve was saturated in 9 hours. Obviously, the final position of the C-V curve depends on the hole trapping probability near the interface. After all holes had reached the interface, a gate-positive field of 1 MV/cm was applied and 5 eV light was used to photoinject electrons from the silicon substrate into the oxide in order to annihilate the trapped holes.

A typical set of C-V curves, all taken at 85°K, is shown in Fig. 4.1. Curve 1 was taken on the fresh sample. Here ΔV is about 0.15 volt, indicating $N_s \sim 3 \times 10^{10}$ cm^{-2}. Not shown in Fig. 4.1 is the effect of a gate-positive bias of 5 MV/cm for 6 hrs. This produced an extremely small shift to the right (∿ 0.05 V), which could be caused by the trapping of $\sim 1 \times 10^{10}$ electrons/cm^2. Curve 2 was measured after exposure at 85°K to soft x-rays for 6 minutes, the gate being biased positively to provide an average field of 1 MV/cm. The ledge shown by the arrow is the result of a small amount of lateral nonuniformity caused by the shadow of the tungsten wire probe on the surface of the field plate during irradiation. The negative shift of Curve 2 indicates approximately 1.6×10^{12} holes/cm^2

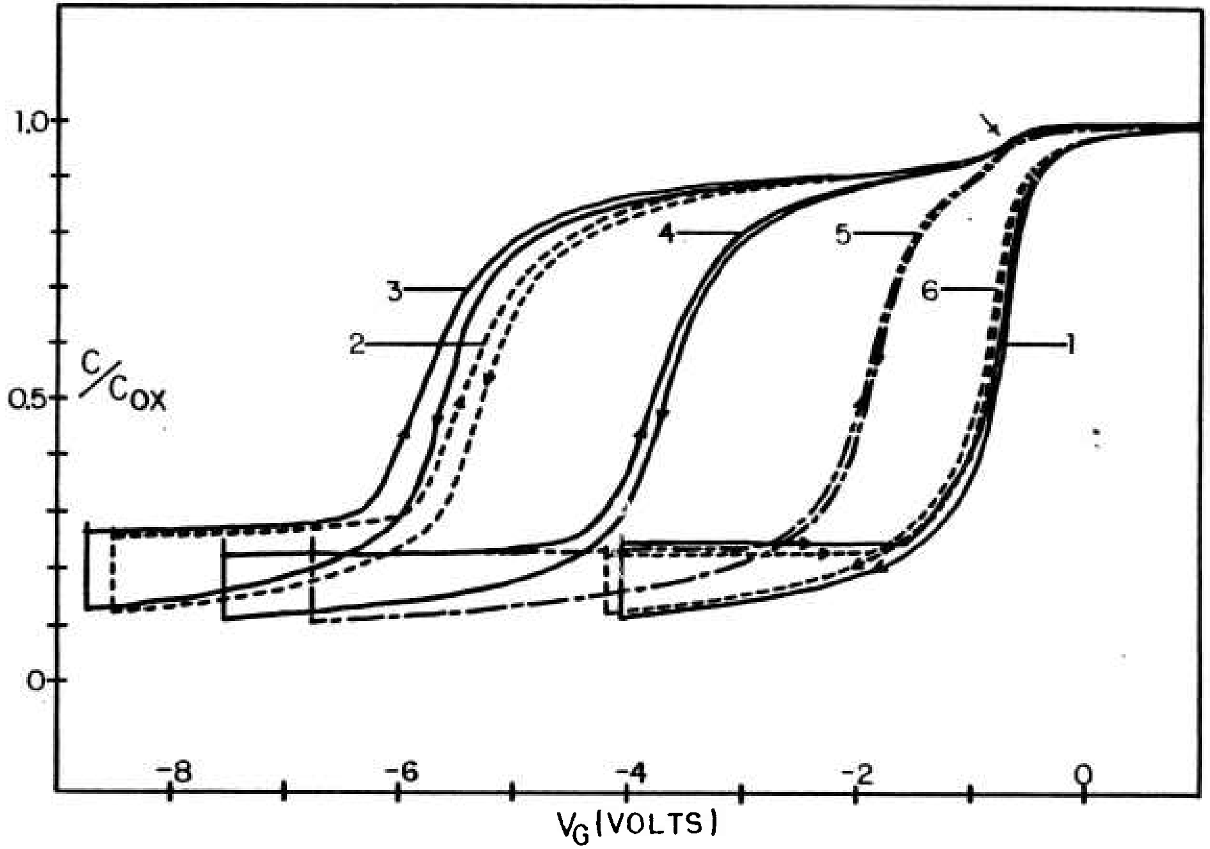

Fig. 4.1 Low-temperature (85°K) C-V curves. (1) Initial condition. (2) After exposure at 85°K to soft x-rays for 6 minutes with 12V gate-positive bias ($\approx$ 1 MV/cm). (3) After +5 MV/cm electric-field stress at 85°K for 9 hours. (4) to (6): The time evolution of the C-V curves after photoinjecting 5.15×10^{12}, 1.39×10^{13}, and 6.11×10^{13} electrons/cm^2, respectively, from Si into the oxide with 5 eV light and + 1 MV/cm electric field. The sample was kept at 85°K throughout all these processes.

trapped in the oxide if the centroid is in the center of the oxide layer. Curve 3 was obtained after application of gate-positive field of 5 MV/cm for 9 hrs to move the holes near the Si-SiO_2 interface. Curves 4 through 6 show the time evolution of the C-V curves when electrons are photo-injected from the silicon substrate to recombine with the holes. The curves were taken after the photoinjection of 5.15×10^{12}, 1.39×10^{13}, and 6.11×10^{13} electrons/cm^2, respectively. The latter corresponds to a charge of $\sim 10^{-5}$ coulomb/cm^2, which, according to the results of Chs. 1 and 2 of this report, is too small to have much effect in generating interface states by passage of electrons. In fact, the number of interface states indicated by the Jenq method is about 2×10^{10} cm^{-2}, which is not much different from the initial value. Curve 6 is at the saturated position, and is slightly to the left of Curve 1. Apparently there is a small amount of positive charge which could not be neutralized by photo-injected electrons.

Figure 2 shows the flat-band voltage recovery as a function of the number of photoinjected electrons measured in the external circuit. From the initial slope of this curve we compute the capture cross section of the trapped holes to be $\sigma = 1.1 \times 10^{-13}$ cm^2, which is in the range typical of a Coulombically attractive center. Curve 3 indicates $p_t \approx 8 \times 10^{11}$ holes/cm^2 presumably trapped near the interface. The product $\sigma p_t = 0.09$ gives the probability in the beginning that an injected electron will recombine with a hole near its point of injection and will not register in the external circuit. The abscissae of the initial data points plotted in Fig. 3.2 should, therefore, be enlarged by the factor $1/(1-0.09) = 1.1$. We have not made this relatively small correction in the figure.

Figure 4.3 shows the 85°K C-V curves obtained after holding the preceding sample at room temperature for 10 days, 28 days, and 91 days, respectively. Interface states, in the amount of about $5 \times 10^{10}/cm^2$, were generated rapidly and remained approximately constant. The C-V curves shifted in a parallel manner to the right and ended somewhat to the right of the original curve (Curve 1 of Fig. 4.1). Some holes may have remained, partially compensated by trapped electrons, in Curve 6 of

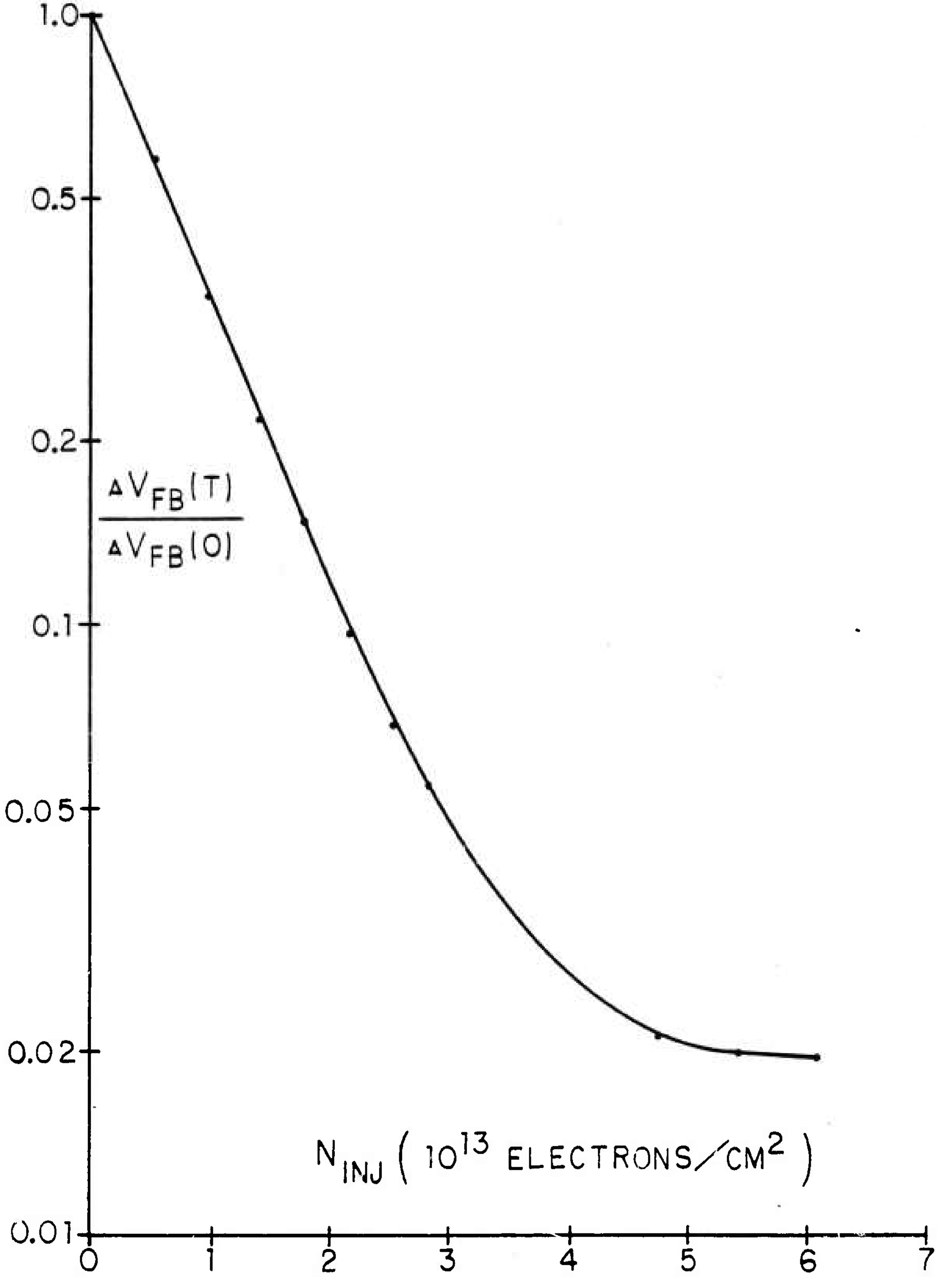

Fig. 4.2 Flat-band voltage recovery as a function of the number of electrons photoinjected at 85°K. The data are normalized to the initial flat-band voltage shift of -4.55 V. The initial slope indicates a capture cross section of 1.1×10^{-13} cm^2.

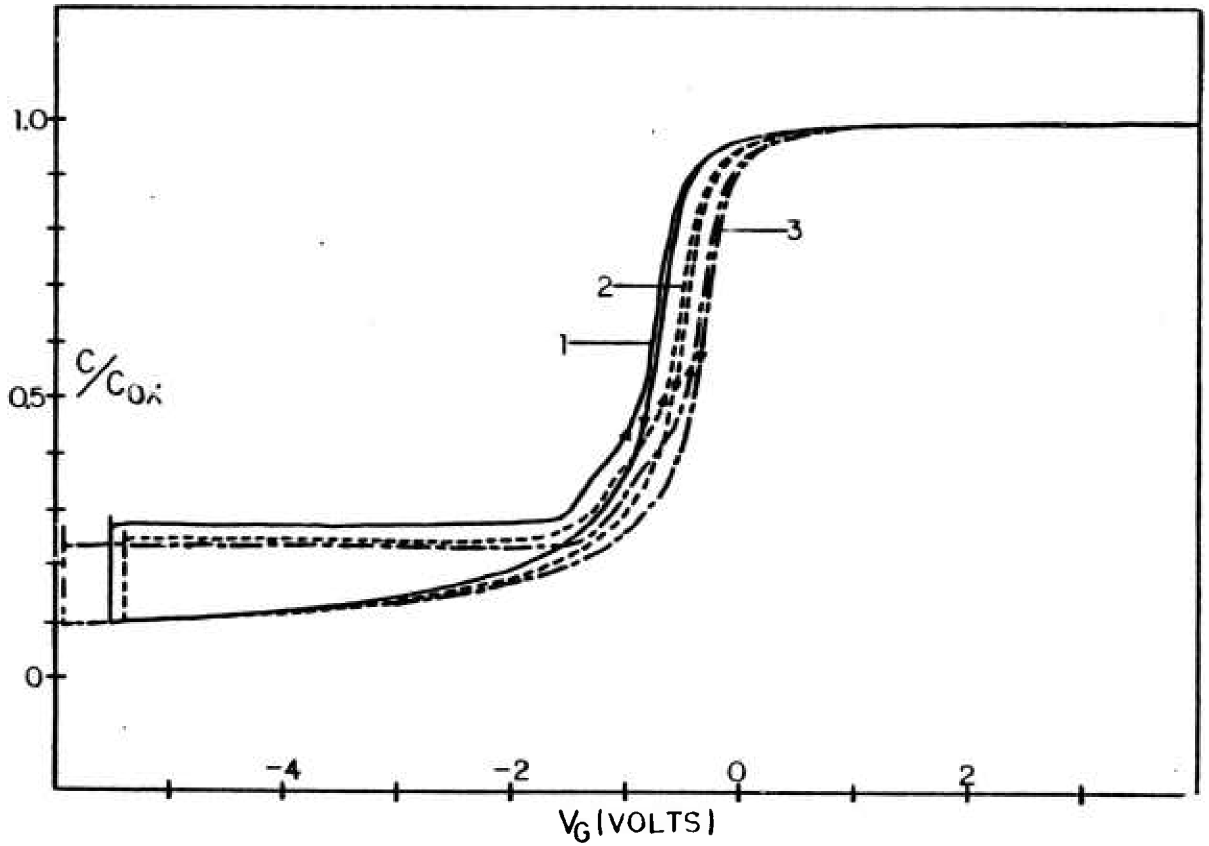

Fig. 4.3 Low-temperature (85°K) C-V curves, taken after the previous sample had been held at room temperature for 10 days, 28 days, and 91 days respectively. The density of interface state is about 5 x 10^{10} cm^{-2}.

Fig. 4.1. Warming to room temperature may have caused the development of interface states, and, in addition, trapped electrons may have been lost (Curve 3 of Fig. 4.3). The effects noted here are not large.

Another sample was subjected to the same processes as have been described above, except that it was warmed to room temperature and held for one hour before the electrons were photoinjected. The C-V curves of Fig. 4.4, which were taken at 85°K, show the results of this experiment. Curve set 1 is the initial deep-depletion and post-illumination curves required for use of the Jenq method. Curve 2 was obtained after soft x-ray exposure due to a nonuniformity. Curve 4 was obtained after the sample had been warmed to room temperature (while open circuited) and held for one hour, then cooled to 85°K. There appears to have been some interface states generated here ($\sim 1.6 \times 10^{11}$ cm^{-2}). Curve 5 was taken after we attempted to annihilate all the holes by photoinjecting electrons (5×10^{13}/cm^2). The density of interface states in Curve 5 appears to be the same as in Curve 4. Curve set 6 shows the result of keeping the sample at room temperature for 60 days. The density of interface states has increased to about 2.3×10^{11}/cm^2. An interesting result in Curve sets 5 and 6 is that in each of these the voltage difference between downsweep and upsweep is divided into two approximately equal portions to the right and to the left, respectively, of the original curve. This is strongly suggestive of equal numbers of acceptor-type and donor-type states, or, more probably, of amphoteric states which can act as both donors or acceptors.

These investigations are continuing.

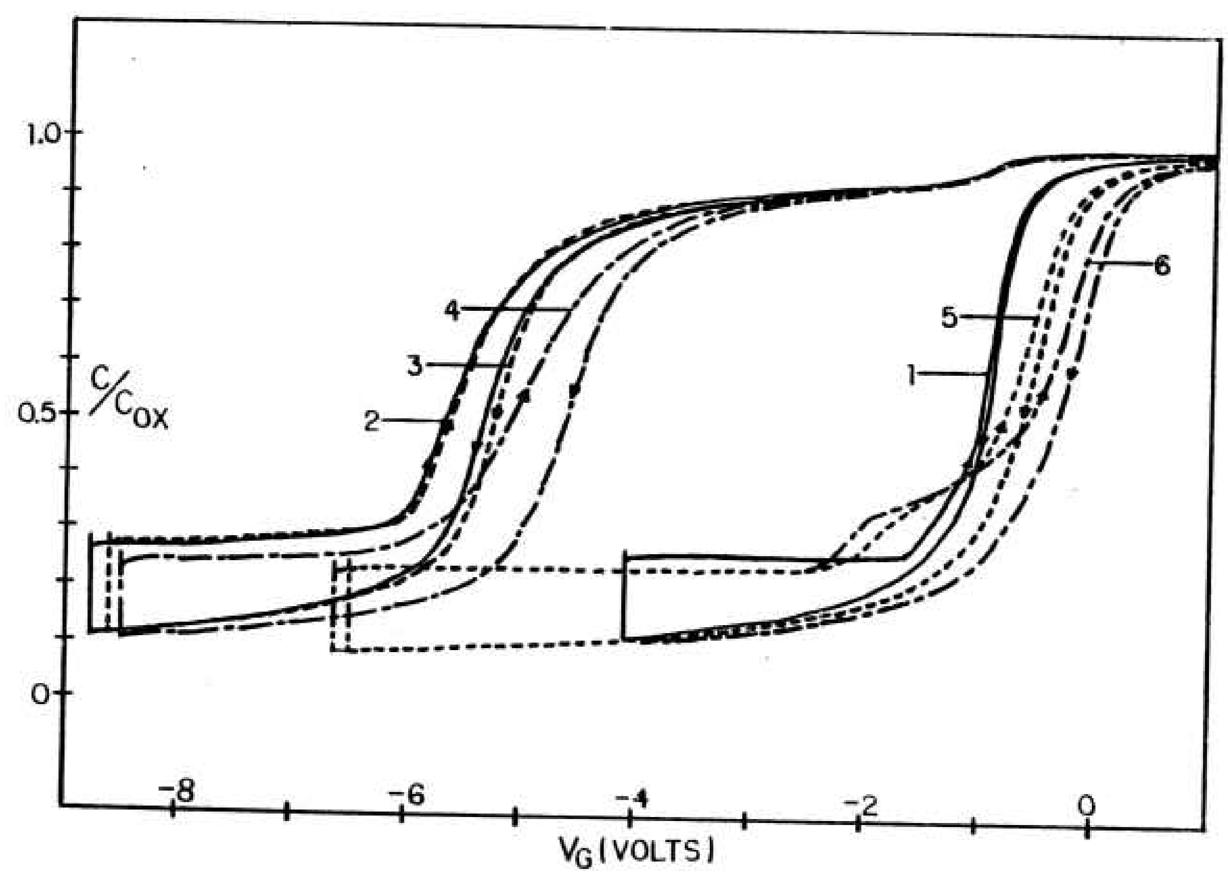

Fig. 4.4 Low-temperature (85°K) C-V curves. (1) Initial condition. (2) After exposure to soft x-rays for 6 minutes with 12 V gate-positive bias. ($\gtrsim$1 MV/cm). (3) After +5 MV/cm electric field stress for 9 hours. (4) After the sample had been open-circuited, warmed to room temperature and held for 1 hour, then cooled to 85°K. (5) After photoinjecting 5×10^{13} electrons/cm^2 from the Si into the oxide with 1 MV/cm electric field. (6) After the sample had been warmed to room temperature and held for 60 days. The density of interface states is about 2.3×10^{11} cm^{-2}.

4.4 References

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